CMS Hadron Calorimeter Front-End Upgrade for SLHC Phase I

Juliana Whitmore [a]
[a] *Fermi Natinoal Accelerator Laboratory, P.O. Box 500, Batavia, IL 60510, USA.*
E-mail: jaws@fnal.gov, Tel: 630-840-5042, Fax: 630-840-2197

We present an upgrade plan for the CMS HCAL detector. The HCAL upgrade is required for the increased luminosity (3 * 10E34) of SLHC Phase I which is targeted for 2014. A key aspect of the HCAL upgrade is to add longitudinal segmentation to improve background rejection, energy resolution, and electron isolation at the L1 trigger. The increased segmentation is achieved by replacing the hybrid photodiodes (HPDs) with silicon PMTs (SIPMs). We plan to instrument each fiber of the calorimeter with an SIPM (103,000 total). We will then electrically sum outputs from selected SIPMs to form the longitudinal readout segments. In addition to having more longitudinal information, the upgrade plans include a new custom ADC with matched sensitivity and timing information. The increased data volume requires higher speed transmitters and the additional power dissipation for the readout electronics requires better thermal design, since much of the on-detector infrastructure (front-end electronics crates, cooling pipes, optical fiber plant, etc.) will remain the same. We will report on the preliminary designs for these upgraded systems, along with performance requirements and initial design studies.

Keywords: CMS, *Hadron, Calorimeter, Front-End, Electronics, Upgrade, SLHC*

1. Introduction

The CMS Hadron Calorimeter [1] is comprised of four distinct subdetectors: the Barrel (HB), the Endcap (HE), the Outer Barrel (HO), and the Forward (HF). The HB, HE, and HO subdetectors are brass scintillator sampling calorimeters with embedded wavelength shifting fibers (WLS). The fibers from the sampling layers are ganged together to form towers whose light is detected by photo-sensors. The photo-sensors that are currently used are hybrid photodiodes (HPDs). The current from the HPD is digitized with a dead-timeless custom ADC operating at 40 MHz. Data from several channels are serialized and sent off the detector via Vertical Cavity Surface Emitting Laser Diodes (VCSELs) onto digital fibers at 1.6GHz [1,2]. This article will focus on an upgrade scenario to the HB and HE front-end readout electronics.

2. SLHC Phase I Environment

The luminosity upgrades to the Large Hadron Collider (LHC) accelerator at CERN will be done in stages. The current plans for Phase 0, the first LHC beam running period, are to have incremental upgrades to the accelerator that result in a peak luminosity of up to 10^{34} $cm^{-2}s^{-1}$. The Phase 1 accelerator upgrade, which will include improvements to the Linac, inner triplets, and interaction regions, is planned to occur after accumulating the equivalent integrated luminosity of $10^{34}cm^{-2}$ (currently estimated to occur around 2014-2016). The expected down period to perform these changes is expected to be ~8 months. With these upgrades, the peak luminosities are expected to be about 2-3 x 10^{34} $cm^{-2}s^{-1}$. The Phase 2 accelerator upgrade plans still are being formulated but might include new injectors and further improvements to the interaction region

that would result in a factor of 3-4 improvement in peak luminosity.

The radiation levels for HCAL through Phase 1, with a delivered integrated luminosity of $10^{34}cm^{-2}$, are expected to be 1.3E11 n/cm^2 and 330 rads in the worst regions (with no safety factors). The HCAL upgraded electronics will be required to survive SLHC Phase 1 (luminosity upgraded to 2-3x$10^{34}cm^{-2}s^{-1}$) and Phase 2 (luminosity upgraded to $10^{35}cm^{-2}s^{-1}$), a factor of 10 more luminosity than the current electronics was tested to survive. With appropriate safety margins, the electronics will need to be radiation hard to the 1E13 n/cm^2 and 10 krad levels.

3. Physics Motivation

High luminosity conditions require improvements to the HCAL detector in order to maintain performance. In the current detector, some regions of HB have a single depth segmentation to its towers. Energy leaking from the electromagnetic calorimeter will damage the inner layers of the HCAL decreasing its response. Adding depth segmentation to the calorimeter towers, at minimum a "Layer 0" forward compartment and a rear compartment, will help improve the energy resolution of the detector. It will also allow the low E_t energy leakage from ECAL to be separated from the high E_t particle flow from jets.

Lepton isolation triggering will be very challenging in SLHC conditions. At a luminosity of $10^{35}cm^{-2}s^{-1}$ with the current HCAL detector design, isolation criteria are insufficient to reduce the Level 1 single electron trigger rate. Current estimates are a 5kHz rate at a E_t trigger threshold of 20 GeV. Simulations have shown that by removing "Layer 0" from the HCAL tower sum, the background rejection is improved.

Higher luminosity will cause severe pile-up conditions. An estimated 200 minimum bias events per crossing (25ns) are expected. In order to reject this out of time energy, improved timing and pulse shape information is required. The time resolution for the current detector is determined by looking at the shape of the pulse integrated over a 25ns time sample. By analyzing the charge sharing between buckets, a +/-1ns time resolution is achieved. But simulations show that pile-up events significantly degrade the pulse-shape determined time resolution. New electronics that includes improved arrival time information will be necessary to reject out-of-time events.

4. The HCAL Front-end Upgrade Design

One goal of upgrading the HCAL sub-detector is to add longitudinal depth segmentation information to achieve better lepton isolation and to improve background rejection. Figure 1 shows

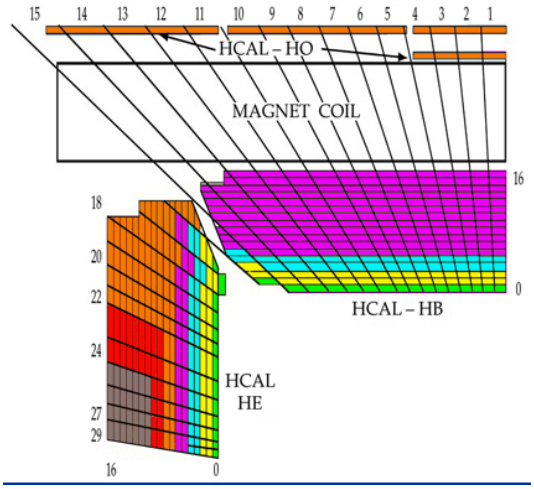

Figure 1: A possible depth segmentation scenario for an upgraded HCAL detector.

one possible layering scenario for HCAL. The colors indicate the depths for the HCAL towers; in this case HB would have 4 depth segmentations. Current upgrade designs are variations on a 4-depth readout design, and would necessitate almost 3-4 times the number of front-end channels. In addition, to upgrade the HCAL detector during the 8 month period of the Phase 1 accelerator shutdown will require much of the existing infrastructure (readout boxes (RBX), digital data fibers, water cooling pipes) to remain the same. Limitations of the existing infrastructure, in particular the space constraints and the electronics cooling, restrict the number of channels to no more than 4 depths. Current readout boxes dissipate roughly 100W of power. The power budget goal for the upgraded electronics will be similar. The higher power chips (e.g. FPGAs and transmitter chips) will be put on boards that will have better thermal coupling to the existing RBX cooling plate.

Currently, the HCAL towers are formed by optically ganging together the wavelength shifting fibers from the tile layers. The plan for the upgraded HCAL has each individual WLS fiber presented to a photo-sensor whose signal is then electrically summed to form the tower depth segments. These Electrical Decoder Units (EDU) will replace the Optical Decoder Uits (ODU) that are currently used in the detector. Figure 2 shows the prototype design of the front plate of the EDU.

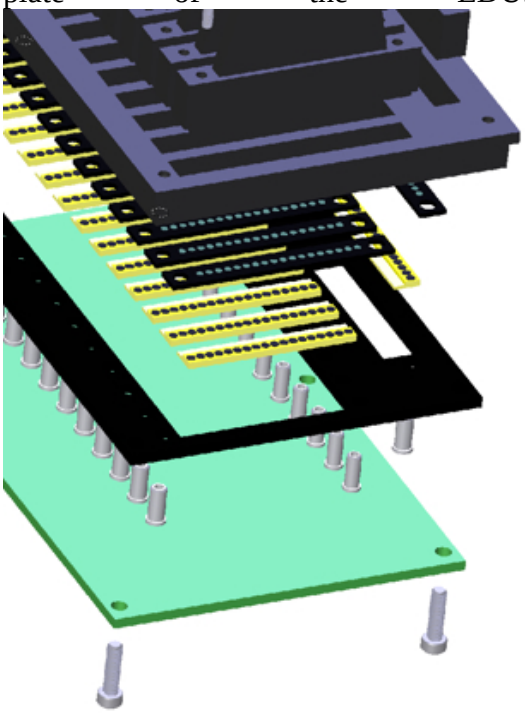

Figure 2: Drawing of the prototype front plate for the EDU.

The photo-sensor technology that is being studied to replace the Hybrid Photodiode in the HCAL is the Silicon PMT (SiPM). These solid-state devices are basically micro-pixilated Geiger mode APDs. They have high gain (10^6), high quantum efficiency (~20%), excellent time resolution, small form factor, can operate in a high magnetic field, can work at room temperature, and can function with a relatively low bias voltage (50-90 V). The devices that seem the most promising for the upgraded HCAL are the Hamamatsu 1 mm x 1mm 1600 pixel Multi-Pixel Photon Counter (MPPC) [3] and Zecotek Micro-Pixel Avalanche Photo Diodes (MAPD) [4] 15,000 pixels 1mm x 1mm individual devices and arrays (1 x 18 arrays). Figure 2 shows a strip of photo-sensors that was used in a beam test at CERN in July.

Figure 3: An 18 srtip SiPM which mates to the analog optical fibers from the HCAL megatiles.

Radiation studies have been performed on the Zecotek (40k cells/mm^2 and 15k cells/mm^2), Hamamatsu (400 cells/mm^2), FBK-IRST (G-APD) (400 cells/mm^2) [5], and CPTA (MRS-APD) (625 cells/mm^2) [6] devices. At 1E12 p/cm^2, the response (normalized to 1E10 p/cm^2) dropped by ~15% for the Zecotek, 70% for the Hamamatsu, and 90% for the CPTA device. The FBK device dropped by 70% after being an 8E11 p/cm^2 exposure.

SiPM gains vary with temperature on the order of 4%-8% per ^{o}C. Peltier coolers will be used to maintain thermal stability of the system. The Peltier system with a slow control feedback loop has been used in a beam test and has been shown to be stable to within 0.1^{o}C.

The current from the SiPMs is then sent to a custom ADC. One ADC option that is being investigated is an upgraded version of the Charge Integrating and Encoding (QIE) [7] ASIC that is currently used for HCAL. The upgraded QIE is a piece-wise linear, dead-timeless ADC that covers an effective dynamic range of 100,000 (16-17 bits) with only 4 range scales (2-bits) for the current-splitter and a 6-bit 5-sensitivity scale FADC. The upgraded chip is a factor of 10 more in dynamic range and 1-bit more sensitive than the current QIE. An additional 2-bits are used to identify the integration capacitor in the 4-stage pipeline. In addition to ADC information, the QIE will generate a TDC bit that will be sent to an FPGA, providing 1-2ns timing resolution. The QIE will also have an programmable adjustment for its integration clock and will synchronize and rephase the digital data going to the FPGA. The processes that are being investigated for the QIE are the AMS 0.8 μm bi-CMOS, the AMS 0.35 μm SiGe bi-CMOS, and the IBM 5AM 0.5 μm SiGe bi-CMOS processes. The advantage of the SiGe processes is the higher radiation tolerance of the bipolar transistors. [6]

The FPGA will function as a controller for the QIE. It will collect, re-phase, reduce redundant data from multiple QIEs, and do simple error checking. The data will be sent to the Gigabit Bi-directional Transceiver chips [8] which will drive 120-bits of data (82-bits of HCAL user-data) onto the fibers at 4.8 Gb/s. Since the number of installed links is limited, the majority of fibers will be used as up-links. A dual optical transmitter using VCSELs is being developed by the CMS Pixel group [9] and would be ideal for the HCAL needs.

Slow controls will also be done via GBT opto-links, with 1 uplink and 1 downlink for slow control communication. The clock, SiPM bias voltages, Peltier Cooler voltages, front-end board voltages, and QIE integration phase adjustment will be downloaded. SiPM leakage current, front-end board voltage read-back, SiPM board and front-end card temperatures will be sent on the uplink.

4. Upgrade Timeline

In order to have upgraded electronics ready to install at the Phase 1 shutdown, the R&D schedule will have to be very aggressive. HCAL is already gaining operational experience with SiPMs from RBXs that were installed in May 2009 in the HO region. The readout modules in these RBXs have 18 SiPMs that replace

the 18 pixel HPDs. Calibration and temperature stability using Peltier cooling is being studied. Figure 2 shows the energy response (sum of 4 time slices) in linearized ADC counts from cosmic rays for an HO SiPM channel.

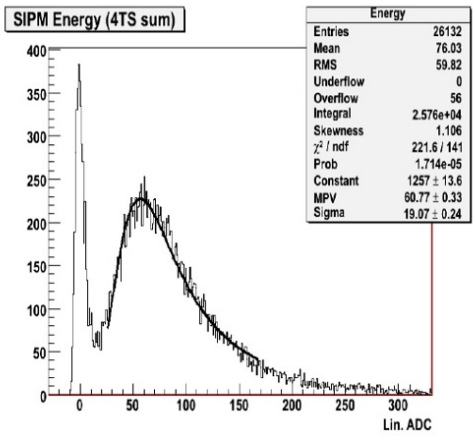

Figure 4: Minimum ionizing particle response for an HO SiPM (sum of 4 time slices) in linearized ADC counts.

CERN beam tests in July 2009 using prototype 4-depth segmentation EDUs have given very promising results. Additional studies of single layer readout are providing information for simulations to better understand the electrical ganging to optimize the energy resolution. Irradiation studies of the SiPMs and support components to SLHC levels are scheduled for Autumn 2009.

5. Summary

An electronics upgrade of the CMS HCAL detector that replaces HPDs with SiPMs is being studied. This upgrade will provide additional depth segmentation information and will improve the detector performance at high luminosity. SiPMs in beam tests and in the HO region of the CMS detector have shown promising results. The HCAL electronics upgrade R&D path is on track for installation during the Phase 1 shutdown.

References

[1] CMS Collaboration, "CMS Technical Design Report, Vol. II: Physics Performance," J. Phys. G34:995-1579, 2007.

[2] T.M.Shaw et al., Proceedings from the IEEEE 2002 Nuclear Science Symposium (NSS) and Medical Imacing Conference (MIC) and Symposium on Nuclear Power Systems, Norfolk, VA, 10-16 Nov., 2002.

[3]Hamamatsu Corp., Hamamatsu Photonics, Shizuoka, Japan. http://sales.hamamatsu.com/en/products/solid-state-division/si-photodiode-series/mppc.php

[4] Zecotek Corp., Zecotek Photonics, Singapore. http://www.zecotek.com/EN/503/1107

[5] FBK, Fondazione Bruno Kessler, Center for Materials and Microsystems, Advanced Photonic and Photovoltaic, Trento, Italy. http://app.fbk.eu/en/home

[6] CPTA, Moscow, Russian Federation. http://www.cpta-apd.ru/eng/APDen.html

[7] Zimmerman, T. and Hoff, J. IEEE J. Solid State Circuits 39: 895-905, 2004.

[8] J. Cressler, Private communication.

[9] P. Moreira (CERN), "The GBT, a Proposed Architecture for multi-Gbps Data Transmission in High Energy Physics," Published in Prague 2007, Electronics for Particle Physics, Sept. 2007.